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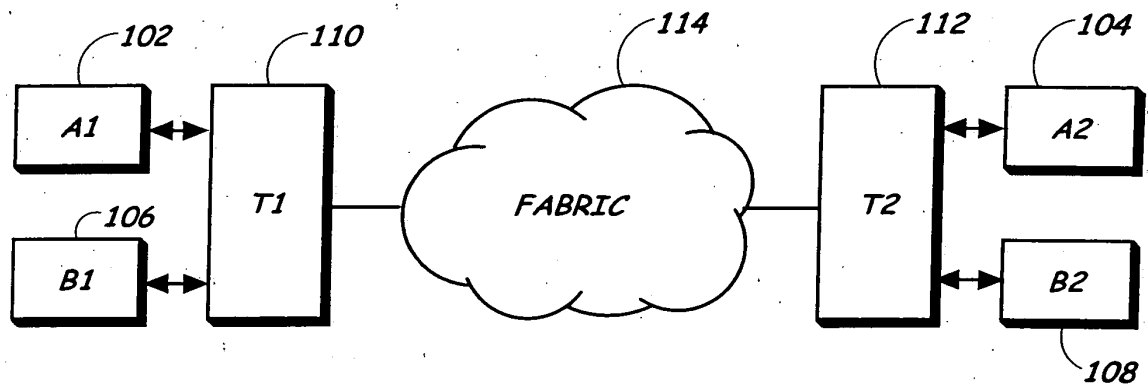
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100

*FIG. 1A*

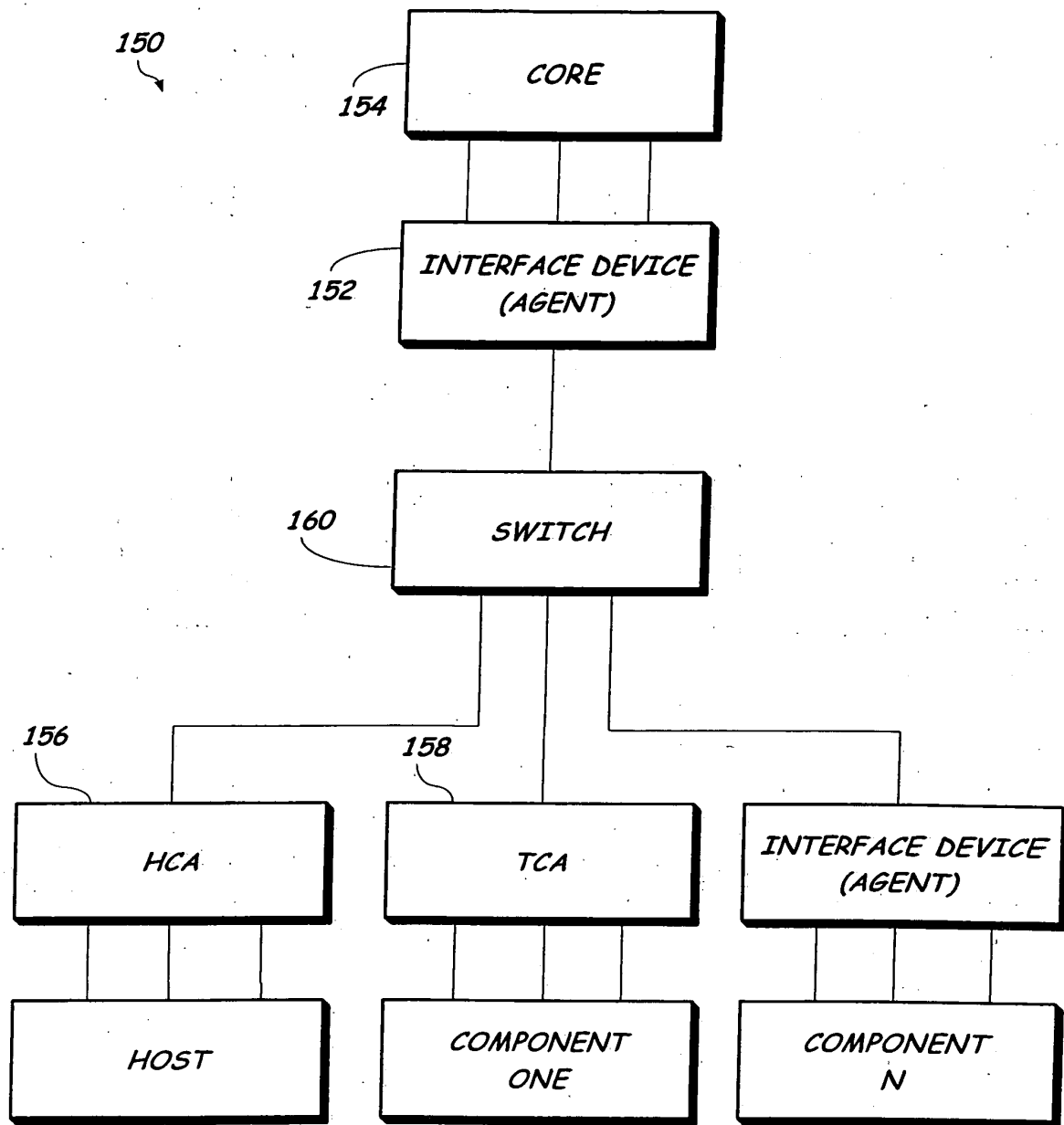
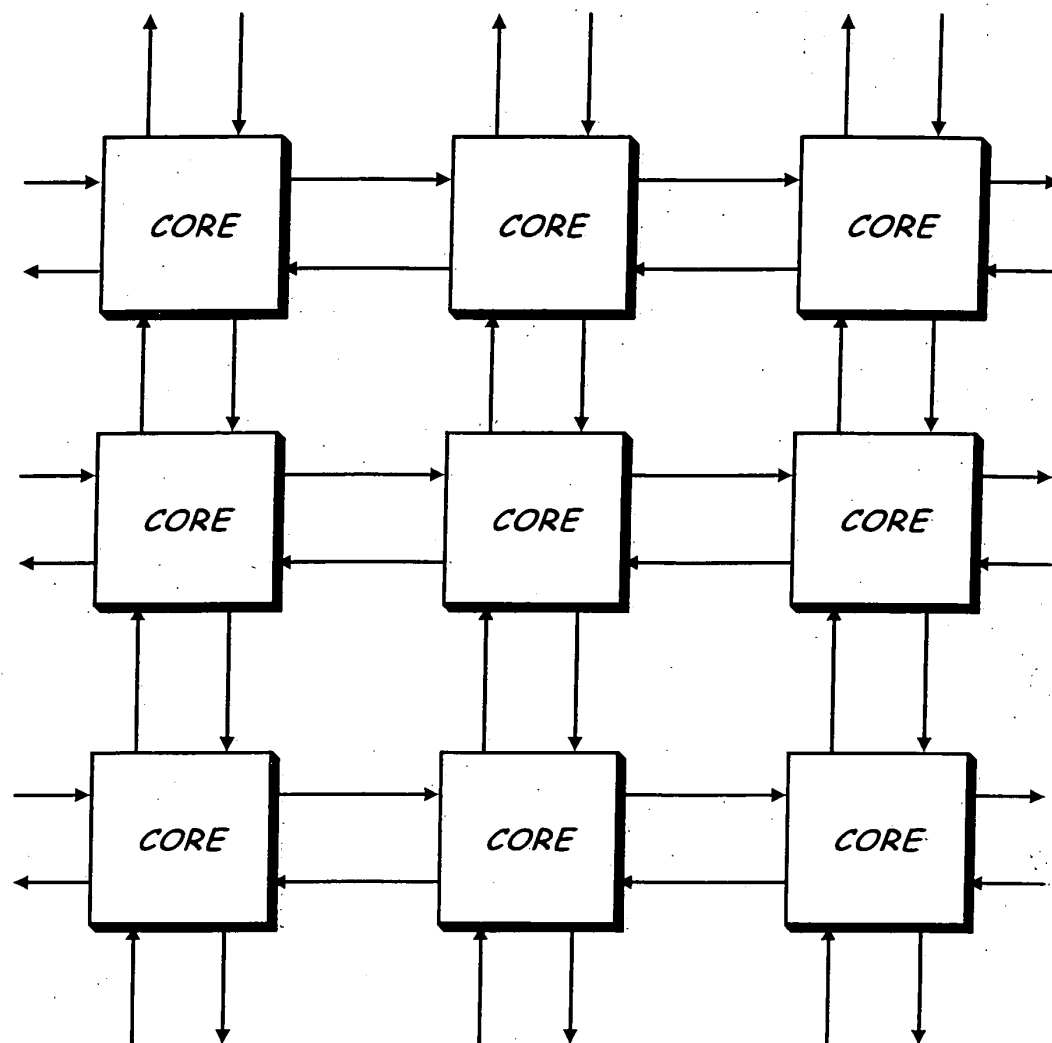


FIG. 1B

*FIG. 1C*

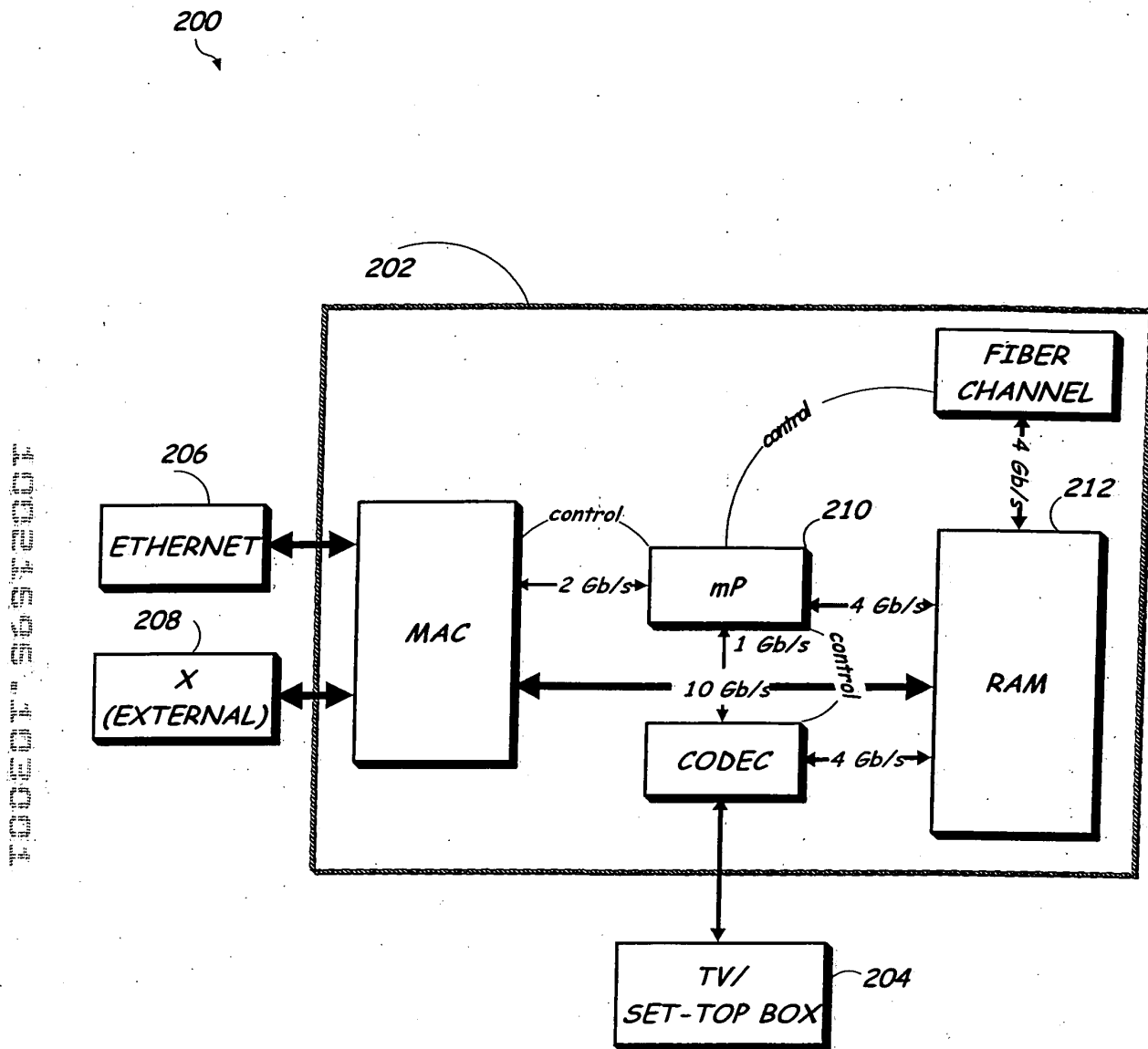
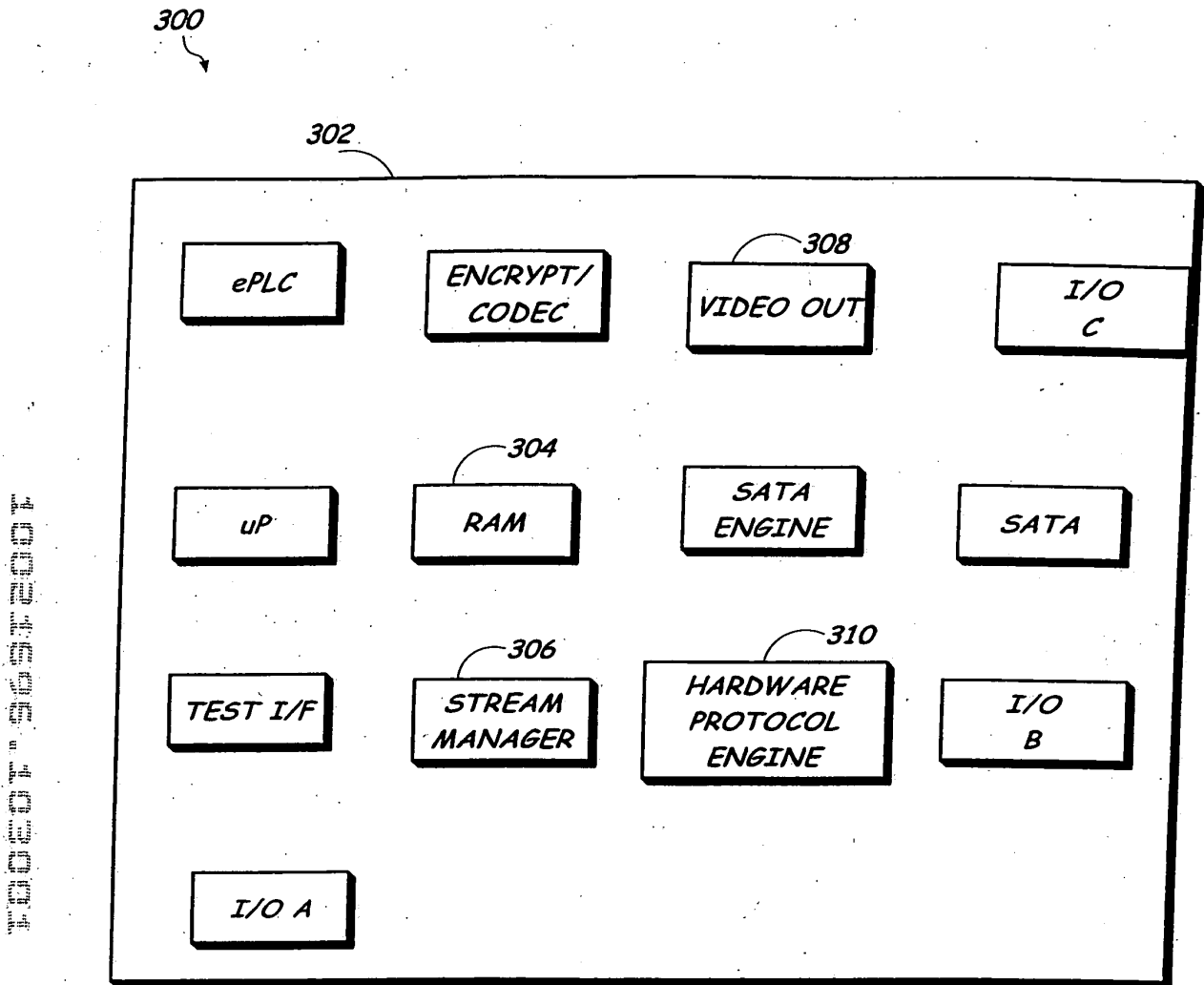


FIG. 2



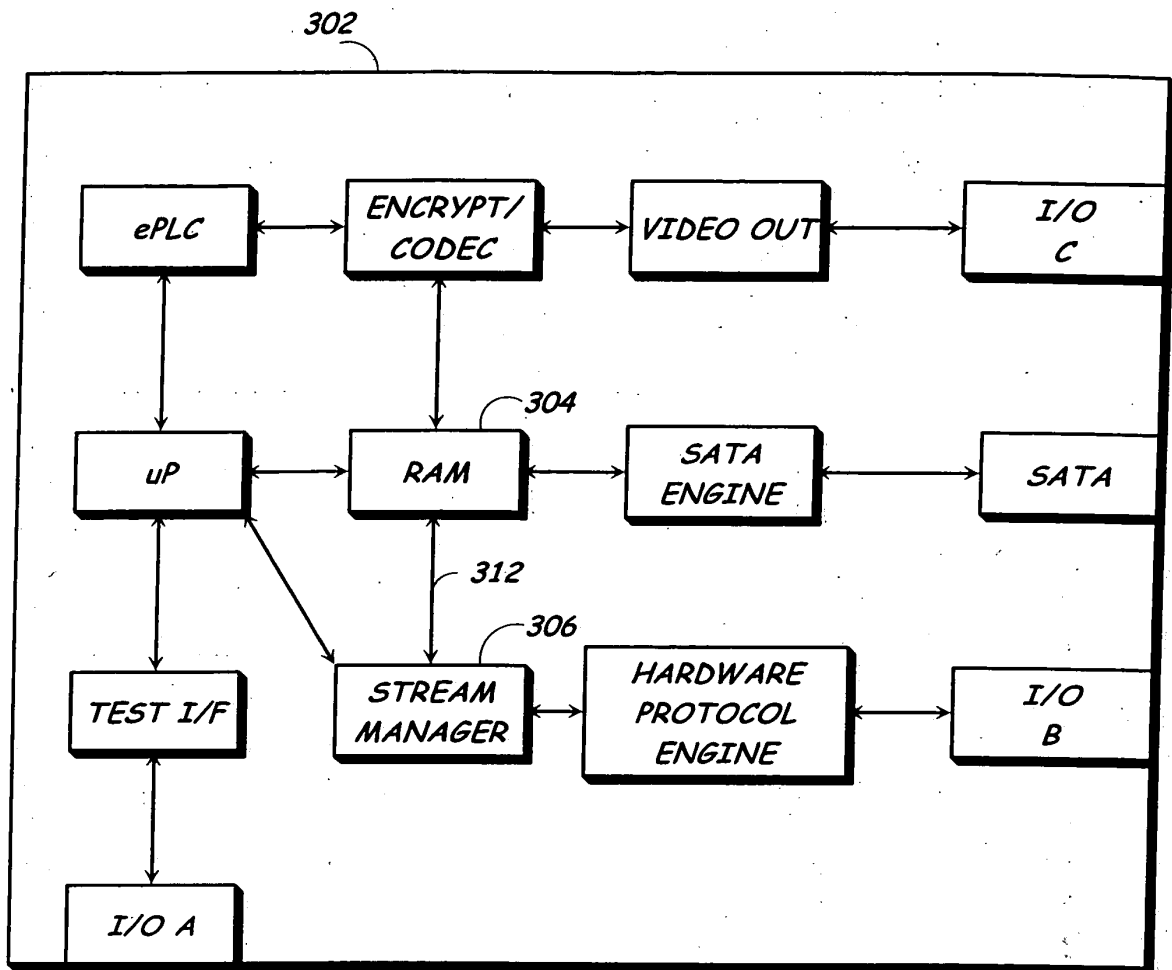


FIG. 4

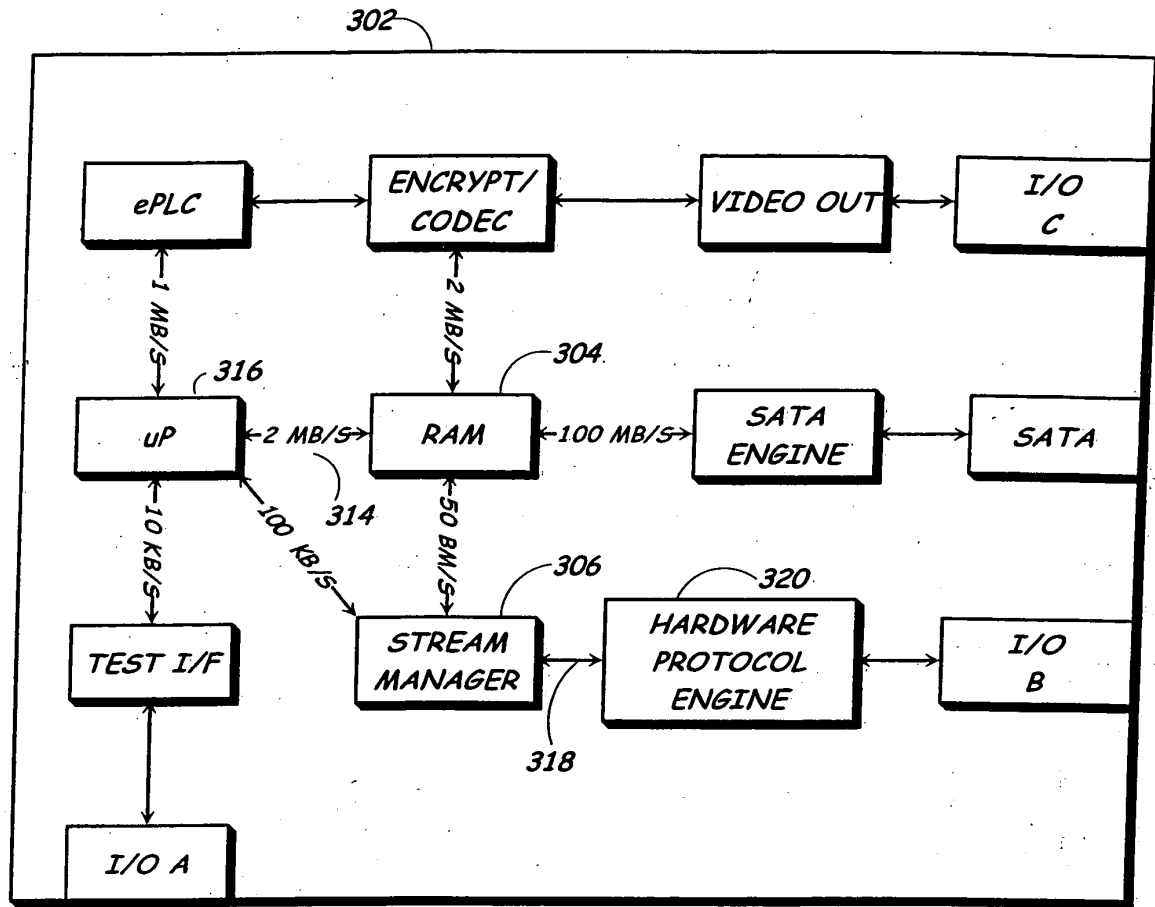


FIG. 5

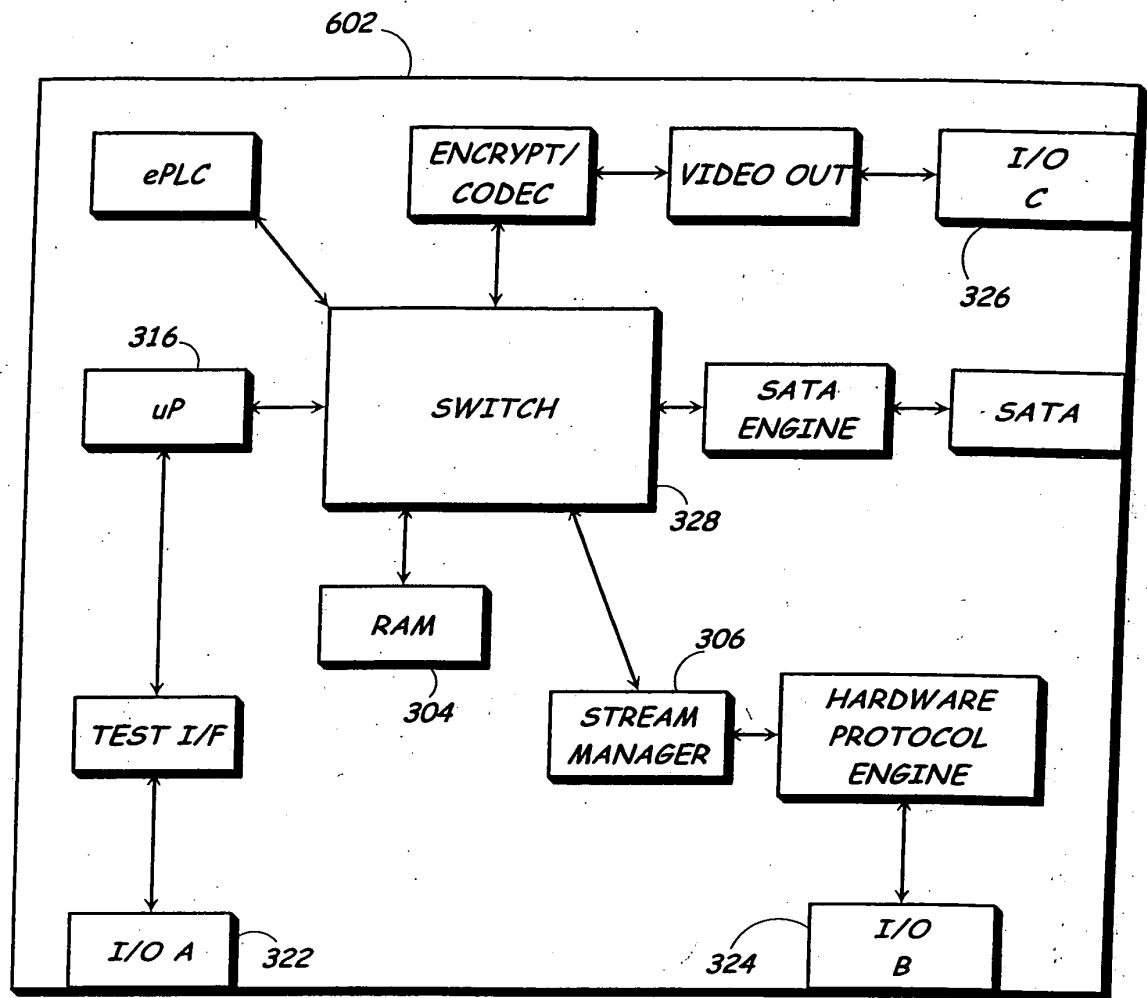


FIG. 6

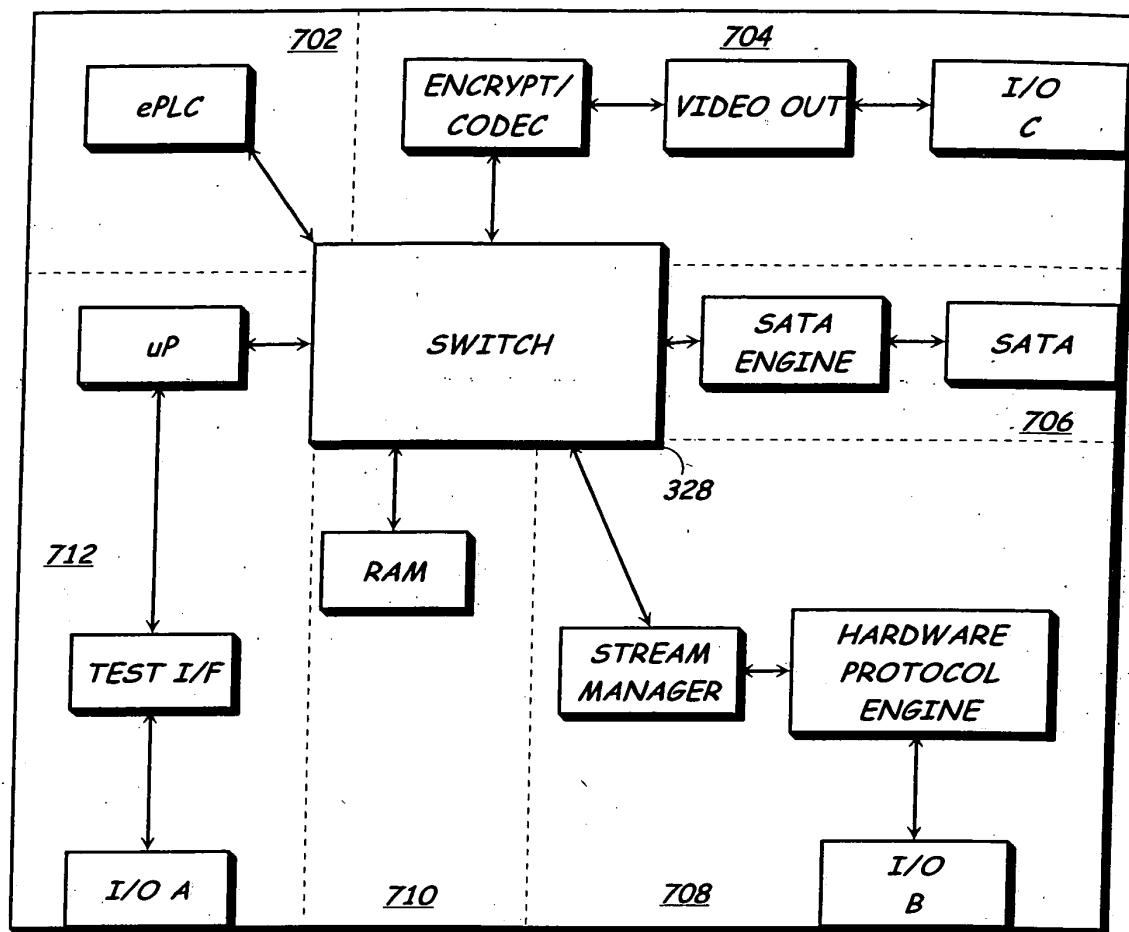
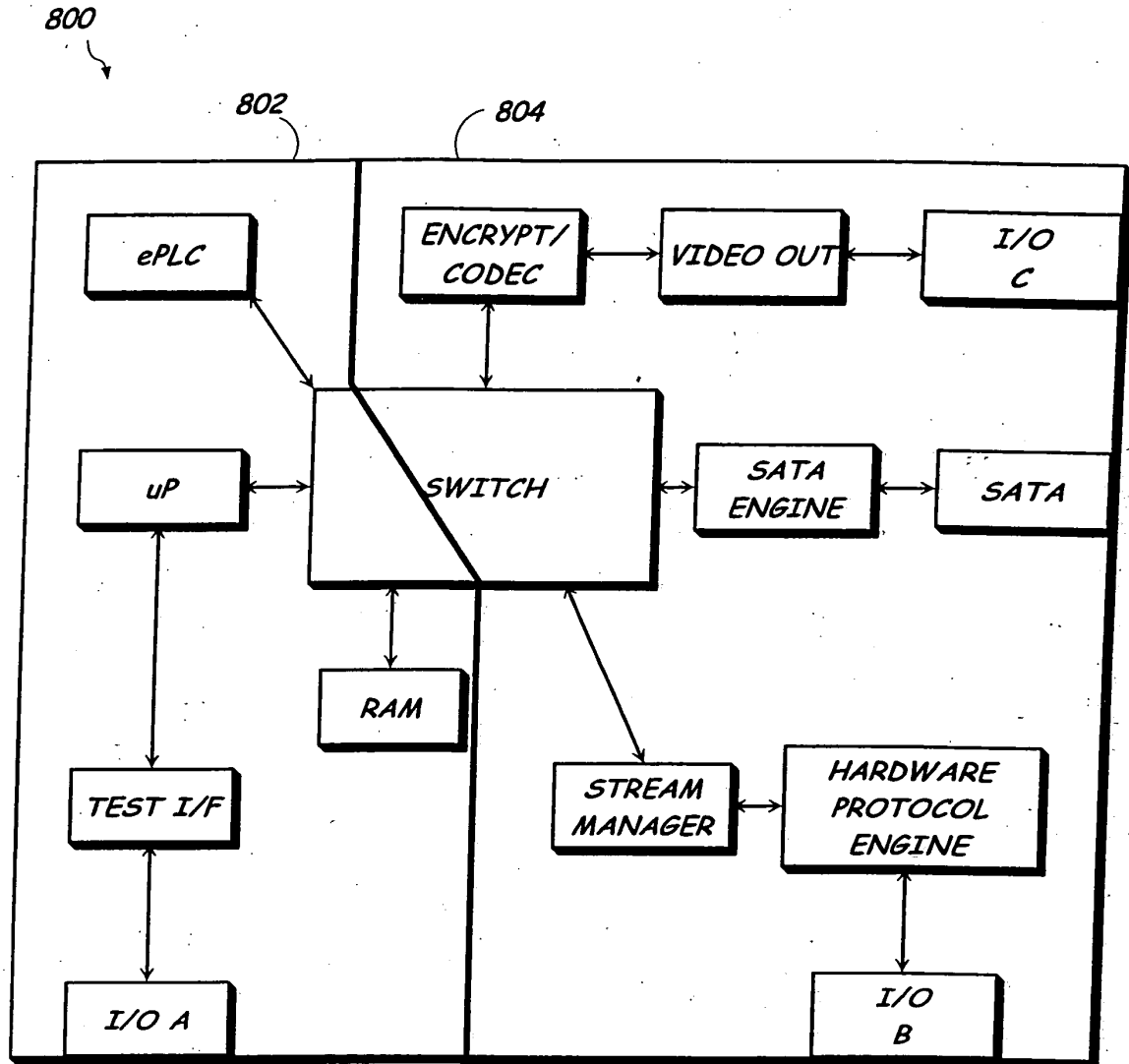


FIG. 7



900

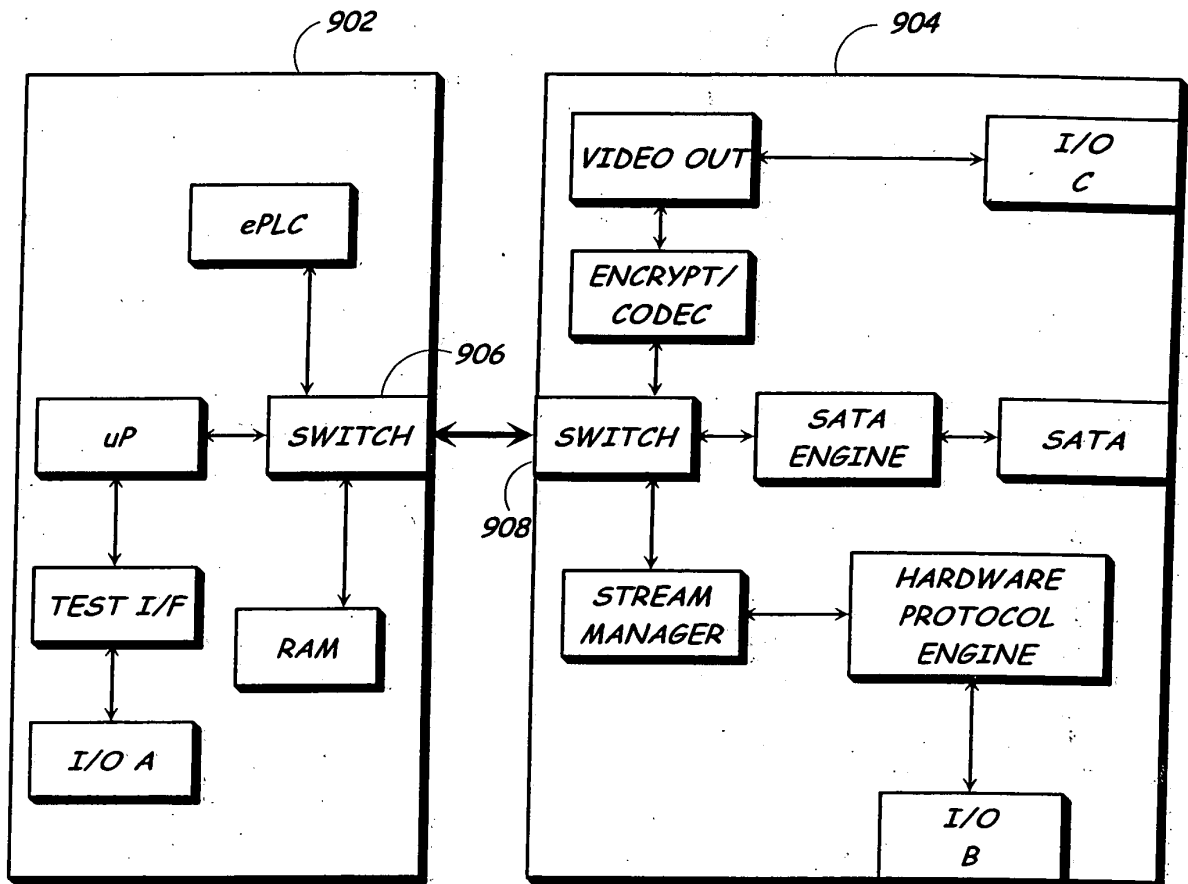


FIG. 9

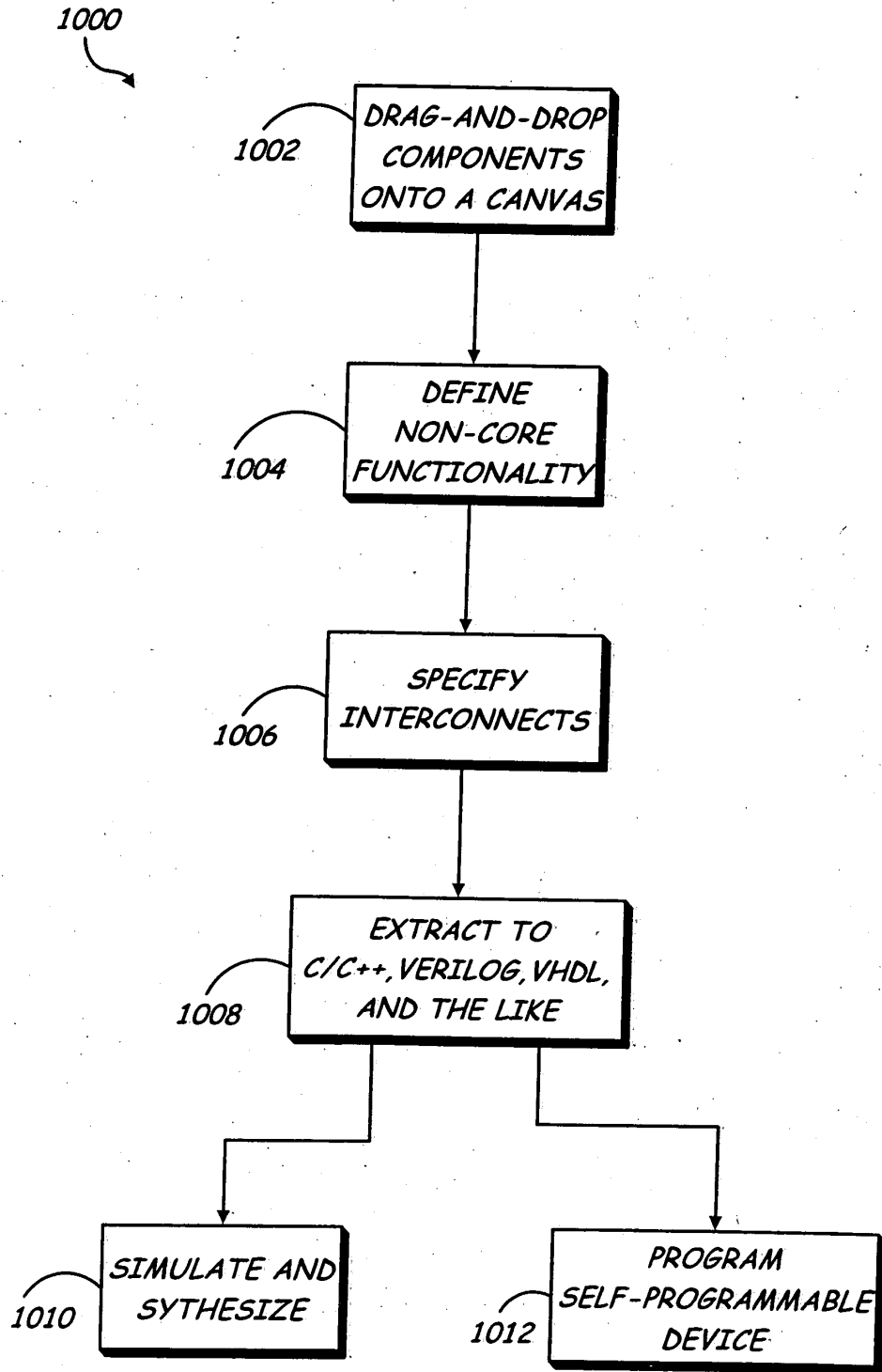


FIG. 10

PROJECT SUPPORT

1100

METHODOLOGY (METASTREAM)

ARCHITECTURAL ENVIRONMENT

1122

CORES, USER FUNCTIONALITY, PARTITIONING, CONNECTIVITY PERFORMANCE,
QoS, POWER PROGRAMMABILITY, AND THE LIKE

EXTRACTION PROCESS

1118

1120

RUNTIME
SOFTWARE
INSTANCE(S)

1114

"SILICON" EXTRACTION

1106

CUSTOM

1108

HARD/SOFT CORES

1110

ePLC MODEL

1112

CuP MODEL

TIMING CONSTRAINTS

1104

1102

SILICON SYNTHESIS

CORES

CUSTOM

CuP

ePLC

INTERCONNECT

← DEVELOPMENT PROCESS →

FIG. 11